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for

NON-OXIDIZING SPACER DENSIFICATION METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICES

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NON-OXIDIZING SPACER DENSIFICATION METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICES

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BACKGROUND OF THE INVENTION

The present invention relates generally to semiconductor devices, and more particularly to metal-oxide-semiconductor ("MOS") devices.

In the manufacture of semiconductor devices conductive polycide is often employed to impart enhanced conductivity to conductive layers. Polycide is a combination of polysilicon and refractory metal silicide layers that offers lower resistivity than polysilicon alone. Polycides may be formed using silicides of a variety of refractory metals including, but not limited to, metals such as titanium, tungsten, tantalum, molybdenum, *etc.* In one common example, the silicidation of polysilicon (*e.g.*, to form polycide) has been previously implemented to reduce the electrical resistance of gate electrode and interconnect metallization in metal-oxide-semiconductor field effect transistor ("MOSFET") devices.

Polycides may be formed in a number of different ways including, for example, by depositing a refractory metal onto a polysilicon layer, followed by annealing at a sufficiently high temperature to form a metal silicide. Alternatively, metal silicide may be deposited, for example, by using sputtering, low pressure chemical vapor deposition ("LPCVD"), evaporation, *etc.* In one example of the latter method, U.S. Pat. No. 5,946,599 describes LPCVD deposition of tungsten silicide onto doped-polysilicon.

Although various methods and improvements thereto have been developed for the fabrication of conductive polycide, problems in the fabrication of polycides still exist. For example, one major problem commonly experienced with existing polycide fabrication technologies is lack of adhesion between the metal silicide layer and the polysilicon layer. This lack of adhesion, or adhesion loss, may result in separation or

peeling of a refractory metal silicide layer from an underlying polysilicon layer, translating to lowered product yield.

Attempts have been made to address adhesion problems encountered with polycide layers, such as those encountered during fabrication of MOSFET devices. For example, U.S. Pat. No. 5,089,432 describes encapsulation of a polycide layer with a tetraethoxysilane ("TEOS") deposited silicon dioxide dielectric layer which is preserved above the polycide layer via masking during spacer etch to improve adhesion. In another example, U.S. Pat. No. 5,946,566 proposes improving adhesion between metal silicide and polysilicon layers by deposition of a polysilicon layer having a wavy or undulated surface, *i.e.*, hemi-spherical grain ("HSG") polysilicon or acid-treated polysilicon. Drawbacks associated with such methods include increased cost and process complexity. Further, encapsulation of polycide requires very tight control of spacer densification conditions, *e.g.*, to maintain a very controlled oxidation environment in a furnace tube, in order to maintain the integrity of the encapsulation.

SUMMARY OF THE INVENTION

Disclosed herein is a non-oxidizing spacer densification method for producing semiconductor devices including, but not limited to, MOSFET devices such as fully integrated complementary metal-oxide semiconductor ("CMOS") devices having non-volatile memory. Advantageously, the disclosed method may be implemented during semiconductor fabrication to provide low cost and robust processes for polycide formation with little or substantially no adhesion loss experienced during spacer oxide densification steps. The disclosed method also makes possible good polycide adhesion characteristics with reduced process complexity over conventional methods by eliminating the need for additional process steps such as metal silicide encapsulation or polysilicon surface treatments. The disclosed method further simplifies the spacer oxide densification step and process sequence since no thermal oxide is grown over the non-volatile memory stack structure, non-memory control gate stack structure and source/drain regions during spacer densification, eliminating the need to manage thermal

oxide growth during this step. Further, the disclosed non-oxidizing method may be used to achieve MOSFET spacer oxide densification while at the same time minimizing or substantially preventing off-site oxide growth loss due to oxidation of exposed silicon surfaces during the densification step.

By employing non-oxidizing species in a MOSFET spacer densification step, the disclosed method surprisingly eliminates the need for the added complexity of a metal silicide top encapsulation layer and the need for controlled oxidation conditions during spacer densification employed in the practice of conventional MOSFET fabrication methods without detrimental effects on the performance of MOSFET transistors. This method of fabrication is contrary to accepted MOSFET spacer densification methodology that employs oxidizing species to grow a thin layer of silicon dioxide in the source and drain areas during spacer densification before, for example, deposition of polysilicon metal dielectric layers.

Thus, in one embodiment, the disclosed method may be practiced to minimize or substantially eliminate undesirable growth of oxidation products (*e.g.*, $W_xSi_yO_z$ on tungsten-based polycide layers) that are believed to result in polycide adhesion loss, and implementation of MOSFET spacer densification in a non-oxidizing environment eliminates the need for encapsulation methods to prevent polycide adhesion loss. Further, the disclosed method makes the spacer etch step substantially completely tolerant or independent of micro-loading effects, *i.e.*, differences in amount of anti-reflective layer that is removed from the top of the polycide layer during spacer etch steps. In this regard, the disclosed method may be successfully practiced under conditions ranging from substantially no removal of anti-reflective layer during spacer oxide etch to almost complete removal of anti-reflective layer during spacer oxide etch (*e.g.*, only a few mono-layers of anti-reflective layer remaining). This characteristic advantageously reduces expense and complexity of the spacer oxide etch step.

Advantageously, the disclosed method may be further implemented in a low cost manner to fabricate high yield and high reliability polycide layers in an existing

MOSFET fabrication unit. In this regard, the disclosed method may be implemented in a manner that reduces necessary capital investment by using existing physical vapor deposition ("PVD") equipment for the sputter deposition of metal silicide, *e.g.*, by addition of a sputter chamber to existing PVD equipment. Additional cost savings may be realized by using rapid thermal processing ("RTP") methodology, *e.g.*, low DT (*e.g.* time at temperature), rather than slow controlled furnace tube oxidizing anneal methodologies that are employed in conventional spacer densification methods. Further cost advantages may be realized using the disclosed method by employing plasma enhanced chemical vapor deposition ("PECVD") for anti-reflective layer ("ARL") deposition rather than using the costlier spin-on deposition of ARL.

In one respect then, disclosed herein is a method of densifying a spacer oxide that at least partially surrounds a polycide structure. The method includes densifying the spacer oxide in a non-oxidizing ambient.

In another respect, disclosed herein is a method of forming a semiconductor structure on a substrate. The method may include forming a polycide structure having at least one polysilicon layer and at least one metal silicide layer, forming a spacer oxide on the polycide structure to at least partially surround the polycide structure, and densifying the spacer oxide in a non-oxidizing ambient to form the semiconductor structure.

In another respect, disclosed herein is a method of forming a non-volatile memory stack structure and a non-memory control gate stack structure of an integrated semiconductor device on a silicon substrate. The method may include forming a dielectric isolation region on the silicon substrate between an active non-volatile memory mesa area and an active non-memory mesa area of the silicon substrate, forming a memory cell oxide layer on the silicon substrate over the active non-volatile memory mesa area, forming a doped floating gate polysilicon layer on the memory cell oxide layer over the active non-volatile memory mesa area, forming an inter-poly oxide layer on the doped floating gate polysilicon layer over the active non-volatile memory mesa area, forming a thin gate oxide layer on the silicon substrate over the active non-memory

mesa area, forming a doped control gate polysilicon layer on the thin gate oxide of the active non-memory mesa area and on the inter-poly oxide layer of the active non-volatile memory mesa area, forming a refractory metal silicide layer on the doped control gate polysilicon layer over the active non-volatile memory mesa area so as to form said non-volatile memory stack structure over the active non-volatile memory mesa area, and forming heavily doped non-volatile memory source/drain regions of the non-volatile memory stack structure in the silicon substrate over the active non-volatile memory mesa area. The method may also include forming a refractory metal silicide layer on the doped control gate polysilicon layer over the active non-memory mesa area so as to form said non-memory control gate stack structure over the active non-memory mesa area, and forming lightly doped non-memory source/drain regions of the non-memory control gate stack structure in the silicon substrate over the active non-memory mesa area. The method may further include forming a spacer oxide side layer on each of the non-volatile memory stack and the non-memory control gate stack structures, densifying the spacer oxide side layers in a non-oxidizing ambient; and forming heavily doped non-memory source/drain regions of the non-memory control gate stack structure in the silicon substrate over the lightly doped non-memory source/drain regions.

In another respect, disclosed herein is a relatively low cost and high yielding method for the integration of tungsten polycide deposition into an existing CMOS fabrication facility. In one embodiment, the method may combine the physical vapor deposition ("PVD") or sputter deposition of a tungsten polycide layer, plasma enhanced chemical vapor deposition ("PECVD") of a silicon oxynitride anti-reflective layer ("ARL"), and rapid thermal processor spacer densification in the presence of a non-oxidizing species (*e.g.*, nitrogen) to produce a non-encapsulated polycide layer having good adhesion characteristics. In this embodiment, RTP in a non-oxidizing nitrogen environment advantageously may be employed to achieve spacer densification without the need for encapsulation methods to prevent polycide adhesion loss.

In another respect, disclosed is a method of fabricating a tungsten polycide interconnection layer in a fully integrated CMOS device having embedded analog

sections and non-volatile memory sections. In one exemplary embodiment, the method may include first depositing a layer of amorphous silicon by, for example, low pressure chemical vapor deposition ("LPCVD"), subsequently doping the deposited layer by, for example, ion implantation, followed by annealing the deposited and doped layer using, for example, RTP to activate the dopant and to reduce damage. The method may next include depositing a tungsten silicide layer on the doped amorphous silicon by, for example, using PVD followed by RTP of the tungsten silicide layer in a nitrogen environment to form a tungsten-based polycide structure. The method may next include depositing a silicon-rich oxynitride layer onto the tungsten-based polycide structure to serve as a polycide ARL for the patterning process using, for example, PECVD deposition. Non-volatile memory and control gate polycide stack structures may next be fabricated, for example, by patterning the tungsten-based polycide structure using photolithography followed by reactive ion etch ("RIE") processes, and a thin oxide may be subsequently grown on the sidewalls of non-volatile memory and control gate polycide stacks, for example, within a furnace tube. Source and drain areas may next be n-doped and/or p-doped to provide desired functionality. The method may next include depositing an oxide spacer layer using, for example, PECVD tetraethyl orthosilicate ("TEOS") deposition. The spacer layer may next be removed and over-etched from the top of the polycide and from the source and drain areas using, for example, RIE. Densification of the spacer and tungsten-based polycide structure may then be accomplished using RTP and a non-oxidizing environment in order to prevent polycide oxidation induced peeling.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simplified partial cross-sectional view of a semiconductor substrate having a dielectric isolation region formed thereon according to one embodiment disclosed herein.

FIG. 2 is a simplified partial cross-sectional view of the semiconductor substrate of **FIG. 1** having a memory cell oxide layer and formed thereon according to one embodiment disclosed herein.

FIG. 3 is a simplified partial cross-sectional view of the semiconductor substrate of **FIG. 2** showing memory cell oxide and doped floating gate polysilicon layers removed from a non-memory mesa area of the substrate; and also showing memory cell oxide layer, doped floating gate polysilicon layer and oxide-nitride-oxide layer formed on a non-volatile memory mesa area of the substrate according to one embodiment disclosed herein.

FIG. 4 is a simplified partial cross-sectional view of the semiconductor substrate of **FIG. 3** having a control gate polysilicon layer, tungsten silicide layer, and anti-reflective layer formed thereon according to one embodiment disclosed herein.

FIG. 5A is a simplified partial cross-sectional view of the semiconductor substrate of **FIG. 4** following patterning, etching and source/drain heavy doping to form a non-volatile memory stack according to one embodiment disclosed herein.

FIG. 5B is a simplified partial cross-sectional view of the semiconductor substrate of **FIG. 5A** following patterning and etching to form a non-memory control gate stack according to one embodiment disclosed herein.

FIG. 5C is a simplified partial cross-sectional view of the semiconductor substrate of **FIG. 5B** following patterning, etching and growth of a thin oxide on the sides of non-volatile memory stack and non-memory control gate stack according to one embodiment disclosed herein.

FIG. 5D is a simplified partial cross-sectional view of the semiconductor substrate of **FIG. 5C** following light doping of source/drain regions of the non-memory control gate stack according to one embodiment disclosed herein.

FIG. 6 is a simplified partial cross-sectional view of the semiconductor substrate of **FIG. 5** following deposition of a spacer oxide layer according to one embodiment disclosed herein.

FIG. 7A is a simplified partial cross-sectional view of the semiconductor substrate of **FIG. 6** following spacer oxide etch and non-oxidizing spacer densification according to one embodiment disclosed herein.

FIG. 7B is a simplified partial cross-sectional view of the semiconductor substrate of **FIG. 7A** following source/drain heavy doping of the non-memory mesa area according to one embodiment disclosed herein.

DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

The disclosed method may be used in the fabrication of any semiconductor device employing a polycide layer and during the fabrication of which a subsequent spacer densification step is employed. Examples of such semiconductor devices include, but are not limited to, MOSFET devices such as memory devices, microprocessors, logic devices, *etc.* Examples of memory devices include, but are not limited to, ROM devices, DRAM devices, SRAM devices, *etc.* Specific examples of non-volatile memory devices include, but are not limited to, EPROM devices, EEPROM devices, one time programmable ("OTP") devices, *etc.* Using the disclosed method, high yielding and reliable MOSFET devices may be manufactured using a spacer densification step performed in the substantial absence of oxidizing species.

FIGS. 1-7 illustrate one exemplary embodiment of the disclosed method that may be employed to produce MOSFET devices having embedded non-volatile memory on a

substrate. As referred to herein, a "substrate" may be any semiconductor substrate including, but not limited to, a semiconductor wafer substrate such as silicon or GaAs. In this regard, a substrate may include a semiconductor wafer or a semiconductor wafer having one or more process layers formed on the wafer. Although the process of FIGS. 1-7 is described with reference to formation of a MOSFET device on a p-type substrate, it will be understood by those of skill in the art that silicon substrate 100 may alternatively be an n-type substrate, and that processing steps (*e.g.*, implantation, dopant types, *etc.*) may be adjusted accordingly to form a MOSFET device thereon.

FIG. 1 illustrates dielectric isolation region 102 formed upon a p-type silicon substrate 100 of a semiconductor device 101. In one embodiment, silicon substrate 100 may have a crystallographic orientation of about 100, although other orientation values are possible. Dielectric isolation region 102 may be formed on substrate 100 using, for example, a conventional selective local oxidation of silicon ("LOCOS") process. In this regard, formation of dielectric isolation region 102 by a LOCOS process may be accomplished, for example, by masking active mesa areas 104 and 106 of silicon substrate 100 and oxidizing exposed area 102 of substrate 100 to grow a thermal oxide 102 on and into the surface of substrate 100, resulting in a sunken silicon dioxide dielectric isolation region 102 surrounded by active mesa regions 104 and 106. As shown in FIG. 1, dielectric isolation region 102 separates active non-volatile memory mesa area 104 from active non-memory mesa area 106. It will be understood with benefit of this disclosure that the disclosed method is not limited to specific LOCOS processes, and may be implemented independent of the specific isolation region characteristics. Further, the isolation region 102 need not be formed by a LOCOS process, but rather may be formed by any other suitable isolation process. For example, a shallow trench isolation ("STI") process as known to those skilled in the art may be employed.

For ease of illustration, an exemplary active mesa area 104 is shown for use in forming memory sections of device 101, and an exemplary active mesa area 106 is shown for use in forming non-memory sections of device 101. However, it will be understood

with benefit of this disclosure by those of skill in the art that it is not necessary that both memory sections and non-memory sections be present, and that benefits of the disclosed method may be realized in the fabrication of any MOSFET device, including devices having only memory sections, only non-memory sections, *etc.* It will also be understood that a wide variety of different MOS type devices may be fabricated using the disclosed method including, but not limited to, CMOS devices, BiCMOS devices, NMOS devices, PMOS devices, *etc.* In this regard, it will be understood that control gate structures having opposite channel conductivity types may be present on the same device to implement CMOS transistor logic. For example, to implement CMOS in the device of the exemplary embodiment of FIGS. 1-7, p-channel transistors (not shown) may also be present on device 101 and formed by use of an n-well implant in p-type substrate 100. It will be understood that in some embodiments it is possible that other structures may be present on a given device, *e.g.*, embedded analog circuits including poly-to-poly capacitors, poly-to-substrate capacitors, and resistors. Further, it will be understood that in other embodiments it is possible that MOSFET control gate structures may be present on a given device to perform a variety of other functions known in the art, *e.g.*, as part of embedded analog capacitor circuitry, *etc.*

As shown in FIG. 2, memory cell oxide layer 108 may be formed by thermally oxidizing the silicon of active mesa areas 104 and 106. Memory cell oxide layer 108 may be of any suitable thickness, however, in one embodiment is grown to a thickness from about 100 to about 350 angstroms thickness, although other thicknesses are possible.

Still referring to FIG. 2, a first amorphous silicon layer may next be deposited as a blanket covering the surface of substrate 100 using, for example, a conventional thermal LPCVD method. Although any suitable deposition temperature and layer thickness may be employed, in one embodiment a deposition temperature of between about 500°C and about 550°C may be used to form an amorphous silicon layer having a thickness of between about 1500 angstroms and about 2500 angstroms. Next, the amorphous silicon layer may be doped with phosphorous or other suitable dopant. In one exemplary

embodiment the amorphous silicon layer may be phosphorous-doped using any suitable method, for example, ion implantation or soaking in $POCl_3$, followed by dopant redistribution and crystallization anneal at suitable conditions to form first doped floating gate polysilicon layer 110, for example, using RTP at a temperature of between about 850°C and about 950°C for a time period of from about 10 seconds to about 20 seconds in a nitrogen environment. Alternatively floating gate polysilicon layer 110 may be deposited directly as polysilicon, for example, by such conventional processes as pyrolyzing silane at an elevated temperature followed by doping, or in yet another alternate embodiment may be deposited directly as doped polysilicon.

Next, doped floating gate polysilicon layer 110 may be patterned, for example, using conventional photolithographic techniques to mask the non-volatile memory section of active mesa area 104. Conventional reactive ion etch ("RIE") or other suitable removal method may be used to remove first doped polysilicon layer 110 where the photoresist pattern is absent, resulting in removal of areas of doped polysilicon layer 110 overlying the non-memory region 106 while leaving a blanket of first doped polysilicon layer 110 overlying the non-volatile memory region 104.

Following patterned etching of floating gate polysilicon layer 110, an oxide-nitride-oxide ("ONO") inter-poly oxide layer 112 may be deposited, for example, using conventional thermal CVD methods, and may be patterned using conventional photolithographic techniques. Next, ONO layer 112 may be removed from non-memory active mesa area 106 using conventional RIE or other suitable removal method. When using a conventional RIE method, ONO layer 112 is removed where the photoresist pattern is absent. Following removal from non-memory active area 106, ONO layer 112 remains in the non-volatile memory region 104 as shown in FIG. 3. Although one exemplary embodiment is described above for forming the structure illustrated in FIG. 3, it will be understood that any suitable alternative methodology may be employed.

Next, a thin gate oxide layer 114 may be deposited, for example, as described in US Pat. No. 6,190,973, which is incorporated herein by reference. In one embodiment,

gate oxide 114 may be thermally grown by oxidation reaction with the silicon of active non-memory mesa area 106 to have a thickness of from about 80 angstroms to about 130 angstroms, although other thicknesses are possible.

A second amorphous silicon layer for the control gate of non-memory and non-volatile memory sections may next be blanket deposited over the surface of semiconductor device 101 using conventional thermal CVD or other suitable method, and in one embodiment may be deposited by thermal CVD to a thickness of from about 1500 angstroms to about 2500 angstroms, although other thicknesses are possible. Following deposition, the second amorphous silicon layer may be doped with phosphorous or other suitable dopant, for example, using ion implantation. A dopant redistribution and crystallization anneal at suitable conditions to form doped control gate polysilicon layer 116 may be processed, for example, using RTP at a temperature of between about 850°C and about 950°C for a time period of from about 10 seconds to about 20 seconds in a nitrogen ambient. Following anneal, surface of control gate polysilicon layer 116 may be chemically cleaned using hydrofluoric acid (HF), standard clean 1 ("SC1") (ammonium hydroxide, hydrogen peroxide and water) and standard clean 2 ("SC2") (hydrochloric acid, hydrogen peroxide and water). As with first doped floating gate polysilicon layer 110, second doped control gate polysilicon layer 116 may be alternatively formed by direct deposition of polysilicon and then doped, or may be directly deposited as doped polysilicon.

Next, a metal silicide (*e.g.*, tungsten silicide or other refractory metal silicide) layer 118 may be deposited on the surface of control gate polysilicon layer 116 using any suitable deposition method. In one embodiment, tungsten silicide layer 118 may be sputter deposited in an argon ambient with a DC bias of from about 1500 watts to about 2500 watts. Any suitable sputter target may be employed, although the sputter target composition in one embodiment may have an atomic ratio of from about 2.5 to about 2.9 silicon atoms to one tungsten atom. Tungsten silicide layer 118 may be deposited to any suitable thickness, in this embodiment to a thickness of from about 500 angstroms to about 2000 angstroms, and alternatively about 1500 angstroms, although other

thicknesses are possible. A crystallization anneal may be processed using RTP at a peak temperature of from about 800°C to about 1100°C, alternatively from about 800°C to a bout 1000°C and further alternatively from about 950°C to about 1050°C, for a time period of from about 30 seconds to about 50 seconds in a nitrogen ambient, although any other suitable temperature, time or combination thereof may be employed. It will be understood that metal silicide layer 118 may alternatively be formed by deposition of refractory metal onto control gate polysilicon layer 116, followed by annealing at a suitable temperature to form metal silicide.

Next, an inorganic anti-reflective layer ("ARL") 120 may be blanket deposited using, for example, a PECVD reactor or other suitable method. Anti-reflective layer 120 may comprise any inorganic material of a thickness suitable for functioning as an anti-reflective layer, including, but not limited to, a silicon rich oxynitride layer deposited to a thickness from about 200 angstroms to about 400 angstroms, alternatively from about 300 angstroms to about 400 angstroms and further alternatively from about 200 angstroms to about 300 angstroms, although other materials and/or layer thicknesses are possible. In one embodiment, value of the optical constant, complex index refraction, for anti-reflective layer 120 is from about 2.50 - 0.50i to about 2.60 - 0.55i, although other suitable optical constant values are possible. FIG. 4 illustrates semiconductor device 101 following deposition of anti-reflective layer 120.

Next, non-volatile memory sections of semiconductor device 101 may be fabricated, for example, first by masking using conventional I-line photolithography methods followed by etching of the memory stack of the non-volatile memory section using a multi-step RIE method that is commonly referred to as "array etch." The array etch may be used to etch the ARL layer 120, metal silicide layer 118, control gate polysilicon layer 116, ONO layer 112 and doped floating gate polysilicon layer 110 into a self-aligned non-volatile memory stack structure using any suitable etching methodology known to those of skill in the art. For example, the array etch may be a single self-aligned etch performed in a single tool using multiple steps that are tuned or directed to specific materials to be etched, or the array etch may be alternatively accomplished using

separate etch steps performed in separate tools or machines for one or more of the separate materials to be etched. Circuit-defining ion implantation steps and conventional sulfuric acid/hydrogen peroxide photoresist removal steps may follow the array etch to form heavily doped source/drain regions 126. In the illustrated exemplary embodiment, heavily doped N+ source/drain areas 126 of p-type substrate 100 may be formed using, for example, arsenic ion implantation or doping with any other suitable N-type dopant. A representation of the resultant non-volatile memory stack is shown overlying non-volatile memory active mesa area 104 of FIG. 5A. As with other ion implantation steps of the disclosed method, heavily doped source/drain regions 126 may alternatively be P+ doped regions as may be required by certain doping schemes described herein, *e.g.*, CMOS, PMOS, *etc.*

Following fabrication of the non-volatile memory section of semiconductor device 101, the non-memory section of semiconductor device 101 may next be fabricated. The non-memory section may also be masked using conventional I-line photolithography methods, and control gates of the non-memory section etched using a polycide RIE method, commonly referred to as "gate etch." Conventional oxygen ash and sulfuric acid/hydrogen peroxide photoresist removal procedures may follow the gate etch. A representation of the non-memory control gate stack is shown overlying non-memory active mesa area 106 in FIG. 5B.

Next, a thin oxide layer 140 may be grown to cover the sidewalls of the non-volatile memory stack and non-memory control gate polycide stack, for example, in a furnace tube with an oxidation temperature of from about 800°C to about 900°C, or under any other suitable conditions. In one embodiment, thin oxide 140 may be grown to a thickness of from about 50 angstroms to about 100 angstroms, although other thicknesses are possible. As illustrated in FIG. 5C, during this step substantially no thin oxide is grown on anti-reflective layer 120. During this step, thickness of gate oxide layers 114 and 108 that remain over the surface of respective active mesa areas 106 and 104 does not substantially change during growth of thin oxide layer 140.

In the illustrated exemplary embodiment, following growth of thin oxide 140 areas of the semiconductor device 101 are masked with photoresist, and then exposed surfaces of semiconductor device 101 may be doped with N and/or P dopants to provide the desired functionality. For example, as illustrated in FIG. 5D lightly doped N- source/drain 122 regions of non-memory active mesa area 106 may be formed in p-type substrate 100 using, for example, ion implantation of N-type dopants such as phosphorous or any doping with any other suitable N-type dopant. Although not shown, it will be understood that in CMOS device embodiments complementary transistors may be formed by lightly doped P- source/drain regions formed in N-well areas of p-type substrate 100 using, for example, ion implantation of P-type dopants such as boron difluoride. Also possible are CMOS embodiments employing n-type substrates having P-wells, with each having source/drain regions doped to achieve the appropriate functionality. Further, with regard to CMOS device fabrication, it will be understood that implantation sequence of N and P dopants may be performed with either of the N or P dopant implantations being performed first.

Following formation of lightly doped source/drain regions 122, spacer oxide 124 may be formed over the surface of semiconductor device 101 as shown in FIG. 6. Spacer oxide 124 may be formed by any suitable method for example, in a PECVD reactor using TEOS as the precursor and oxygen as the oxidant. In one embodiment, spacer oxide 124 may be deposited to a thickness of from about 1200 angstroms to about 2000 angstroms, alternatively from about 1200 angstroms to about 1600 angstroms and further alternatively from about 1400 angstroms to about 1600 angstroms, although spacer oxide 124 may be formed to have any other suitable thickness outside this range.

Following deposition of spacer oxide 124, an RIE blanket etch or other suitable removal method may next be performed to remove spacer oxide from non-volatile memory active mesa area 104 and non-memory active mesa area 106, leaving spacer oxide side layers 132. In one embodiment, a conventional CF_4/CHF_3 oxide etch may be performed using a standard oxide etch tool. In this embodiment, the etch is end-pointed when the oxide is removed from active areas 104 and 106, followed by over-etching (*e.g.*,

over-etch of about 25 percent), resulting in exposed source and drain areas 122 and 126 as shown in FIG. 7A. As may be seen in FIG. 7A, the RIE blanket etch also is performed to remove material of spacer oxide layer 124 and to optionally remove material of ARL layer 120 from the upper surfaces 130 of the non-volatile memory stack and the non-memory control gate stack, for example, leaving all or part of layer 118 exposed. In this regard, it will be understood that upper surfaces of layer 118 may be completely exposed due to total removal of layer 120, or that all of portions of layer 120 may remain (*e.g.*, after spacer oxide etching layer 120 may have a thickness ranging from about 0 angstroms to substantially unetched original thickness), and that any remaining portions of layer 120 may vary in thickness across upper surfaces 130 of the non-volatile memory stack and the non-memory control gate stack.

Following spacer etch, spacer oxide side layer 132 is densified in a non-oxidizing environment, and without encapsulation of upper surfaces 130 of the non-volatile memory stack and the non-memory control gate stack. Using the disclosed method, spacer densification may be accomplished in the presence of any non-oxidizing ambient species or combination thereof suitable for achieving spacer oxide densification under the conditions required therefor. In one embodiment, the term "spacer densification" may be used to describe exposure of spacer oxide side layers 132 to conditions that include temperature and time sufficient to densify the oxide material in the spacer oxide side layers 132 by increasing the number of Si-O bonds that exist in the deposited oxide (*e.g.*, such as the initially loosely bonded molecular structure of TEOS-deposited oxide). Because the densification is performed in a non-oxidizing ambient, substantially no oxide is grown in the exposed surfaces of non-memory active mesa area 106 and non-volatile memory active mesa area 104, as is the case with conventional spacer densification methodology.

Examples of suitable non-oxidizing species for spacer densification include, but are not limited to, nitrogen, argon, helium, deuterium, combinations thereof (*e.g.*, nitrogen/argon mixture), *etc.* Spacer oxide densification may be performed using any suitable method for exposing the spacer oxide side layers 132 to elevated temperatures

sufficient for densification. In one embodiment, the spacer oxide may be densified using RTP in a nitrogen ambient at a temperature of from about 850°C to about 1050°C, alternatively from about 900°C to about 1050°C, further alternatively from about 850°C to about 950°C and further alternatively from about 900°C to about 950°C for a time period of from about 10 seconds to about 30 seconds, alternatively from about 15 seconds to about 30 seconds, although any other temperature, time, or combination thereof may be employed. Alternatively, densification may be performed in a standard furnace tube in a non-oxidizing ambient (*e.g.*, nitrogen, argon, helium, deuterium, combinations thereof, *etc.*) or in yet another exemplary embodiment, may be performed in a modified RTP under vacuum.

Following spacer densification, heavily doped source/drain regions 142 may be formed in non-memory active mesa area 106 as shown in FIG. 7B. In the illustrated exemplary embodiment, heavily doped N+ source/drain areas 142 may be formed using, for example, arsenic ion implantation or doping with any other suitable N-type dopant. As with other ion implantation steps of the disclosed method, heavily doped source/drain regions 142 may alternatively be P+ doped regions as may be required by certain doping schemes described herein, *e.g.*, CMOS, PMOS, *etc.* Because substantially no oxide is grown in the exposed surfaces of active mesa area 106 during spacer densification, greater control over ion implantation may be advantageously achieved.

Although one exemplary embodiment of the disclosed method using a non-oxidizing spacer densification step to fabricate a CMOS device having embedded non-volatile memory sections has been described above, it will be understood with benefit of the present disclosure that benefits of the disclosed method may be realized in the fabrication of any semiconductor device having one or more conductive polycide structures and that may be subjected to one or more MOSFET spacer densification steps including, but not limited to, other types of CMOS devices, BiCMOS devices, NMOS devices, PMOS devices, *etc.* Furthermore, it will be understood that the number and type of fabrication steps may vary, and that benefits of the disclosed non-oxidizing spacer densification methodology may be realized using fewer, additional, and/or alternative

process steps (including alternative processing conditions) as disclosed in the exemplary embodiment above.

Thus, for example, although particular exemplary embodiments have been illustrated and described herein, it will be understood that source/drain regions 122 and/or 126 of a MOSFET device may be N doped or P doped, as necessary to achieve the desired functionality or functionalities of a semiconductor device 101. In this regard, source and drain regions 122 and/or 126 may be doped with an impurity type different from the type of impurity present in substrate 100 under a respective gate structure. For example, both P channel and N channel MOS devices may be manufactured using the disclosed method, and source/drain regions 122 and/or 126 may be either P doped or N doped accordingly. Alternatively, both P channel and N channel devices may be present on the same semiconductor substrate 100 of semiconductor device 101 as in the manufacture of CMOS devices. Thus, it will be understood that the disclosed process may be employed to manufacture any type of MOSFET device in which polycide may be employed or present including, but not limited to NMOS, PMOS, CMOS, BiCMOS, etc.

In one embodiment, optional additional thermal treatments may be employed to reduce sheet resistance of a metal silicide (*e.g.*, tungsten silicide layer) to a desired value, in one embodiment to a value of from about 6.5 ohms/square to about 9.0 ohms/square. For example, a combination of RTP steps may be employed for this purpose, including RTP steps performed for other purposes such as densification of plasma-deposited insulating oxide layers. With benefit of this disclosure, those of skill in the art will understand that the sequence or combination of such RTP steps should be managed to avoid forming a grain structure, crystalline structure and/or stochiometry that is too difficult to etch using dry-etch methods. It will be further understood that the sequence or combination of such steps should be managed to reduce phosphorus migration from the underlying polysilicon layer into the tungsten silicide layer which may adversely affect the work function character of the control gate.

In another embodiment, a tungsten polycide process may be implemented in an existing CMOS fabrication facility in the following manner. A PVD tungsten silicide chamber may be added to an existing cluster-tool (e.g., an Applied Materials ENDURA platform). Such a chamber may use a single tungsten silicide target with a specific Si:W ratio consistent with the desired ratio for the deposited layer, for example, a ratio of from about 2.5:1 to about 2.9:1. One example of such a target is manufactured using powder metallurgy and using, for example, Hot Iso-Static Press ("HIP") and hot press methods. In one exemplary embodiment, such a target may be manufactured from the HIP method so as to achieve 100% nominal density, and to have a structure within the centered target shape that is a matrix of tungsten silicide crystal grains and silicon grains with general grain size of about 50 microns. It will be understood that the foregoing description of tungsten silicide chamber and tungsten silicide target are exemplary only, and that the disclosed method may be employed with other types of tungsten silicide deposition equipment and/or methods, including those described elsewhere herein.

Thus, while the invention may be adaptable to various modifications and alternative forms, specific embodiments have been shown by way of example and described herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims. Moreover, the different aspects of the disclosed method and structures may be utilized in various combinations and/or independently. Thus the invention is not limited to only those combinations shown herein, but rather may include other combinations.